

CLAIMS

What is claimed is:

1. A recording/reproducing apparatus comprising;
a data scrambler having a random data generator for generating random data in a cycle of 32 KB in order to scramble data having structure of 2 KB for a sector or a data frame and 64 KB for an ECC block.
2. The apparatus of claim 1, wherein the random data generator comprises:
a 15-bit serial register r_0 through r_{14} for generating the random data by shifting left synchronized with a clock input for scrambling; and
an exclusive OR gate for outputting an exclusive OR value exclusive-ORing output from a higher-most register r_{14} and output from a lower register r_{10} to a lower-most register r_0 ,
wherein the scrambler includes an exclusive OR logic circuit which supplies a result of exclusive-ORing 1-byte input data D_0 through D_7 and each of the 8 outputs of lower registers r_0 through r_7 after left-shifting the 15-bit register r_0 through r_{14} 8 times.